

Abstract

Proposed is a control unit featuring clocked data transmission between a processor (μ C) and at least one further circuit (ASIC 1, 2, n), the processor (μ C) itself outputting the clock pulse (SCKr). The processor (μ C) monitors the clock pulse (SCKr) based on the output signals of 5 at least two clock outputs (10, 11).

(Figure 1)